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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,464	04/08/2004	Graeme Storm	02EDI46652637	7257

27975 7590 12/26/2008

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EXAMINER	
QUIETT, CARRAMAH J	
ART UNIT	PAPER NUMBER
2622	

NOTIFICATION DATE	DELIVERY MODE
12/26/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

creganoa@addmg.com

Office Action Summary	Application No.	Applicant(s)	
	10/820,464	STORM ET AL.	
	Examiner	Art Unit	
	Carramah J. Quiett	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14,17-23,27-31 and 34-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14,17-23,27-31 and 34-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment(s), filed on 09/25/2008, have been entered and made of record. Claims 14, 17-23, 27-31 and 34-36 are pending.

Response to Arguments

2. Applicant's arguments filed 09/25/2008 have been fully considered but they are not persuasive.

In the Remarks filed 09/25/2008, the Applicants asserted that Morris et al. does not disclose the second output switch as recited in amended independent Claim 14. The Examiner respectfully disagrees. Please note that the second output switch in Claim 14 is recited as,

> "...said second output circuit comprises:
> an amplifier, and
> a log select switch for connecting said amplifier to said photodiode..."

In figures 3 and 4, Morris illustrates the second output circuit as recited in Claim 14. In col. 4, lines 30-54, Morris teaches inherently teaches an amplifier, the source follower 156, which receives an intensified pixel voltage V_{PD} from a sampling node 160. As taught by Morris, the image sensor/pixel in figures 3-4 is able to be switched from linear mode and logarithmic mode via a MOSFET 150. When the logarithmic mode is asserted, a voltage V_G is applied to the MOSFET 150 and then the node 160, which serve as the log select switch. The source of MOSFET and the sampling node 160 connects the source follower 156 to the photodiode 152. Please see fig. 4 and read col. 4, lines 30-54; and col. 5, line 35 – col. 6, line 51.

As stated by the Applicants, Claims 21 and 31 are similar to Claim 14. Therefore, please refer to the response to Claim 14 for Claims 21 and 31. Accordingly, the Examiner respectfully

maintains the rejections to independent pending Claims 14, 21, and 31 as well as the rejections to the dependent pending claims.

Claim Rejections - 35 USC § 102

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. **Claims 14, 21-23, 25-26 and 31** are rejected under 35 U.S.C. 102(e) as being anticipated by Morris et al. (U.S. Pat. #6,697,112).

For **claim 14**, Morris discloses an image sensor (fig. 3, ref. 140), comprising:

an array (119) of pixels, each pixel (fig. 4) comprising

a photodiode (152, col. 4, lines 3-29),

a first output circuit (figs. 3, 5, 6,7, 8) for deriving a linear output signal by applying a reset signal to said photodiode and reading a voltage on said photodiode after an integration time, said first output circuit comprising

a reset switch (fig. 3, refs. 124/129) for applying a reset voltage to said photodiode (col. 4, lines 3-29), said reset switch comprising a reset transistor (fig. 4, ref. 150) including a conducting terminal connected to said photodiode (col. 6, lines 32-51), and

a readout switch (fig. 3, refs. 124/129) for turning on the conducting terminal of said reset transistor after expiration of the integration time (col. 4, line 55 – col. 5, line 25; col. 6, lines 8-51). (col. 4, line 55 – col. 5, line 25; col. 6, lines 32-51),

a second output circuit (figs. 3, 9, 10, 11, 12) for deriving a logarithmic output signal by reading a near instantaneous illumination-dependent voltage on said photodiode that is a logarithmic function of the illumination (col. 5, lines 34-55), said second output circuit comprises:

an amplifier (fig. 4, ref. 156/160; col. 4, lines 3-54), and

a log select switch (fig. 4, refs. 150/156) for connecting said amplifier to said photodiode (col. 4, lines 30-54; col. 5, line 35 – col. 6, line 51), and

said first and second output circuits sequentially providing the linear and logarithmic output signals (col. 6, lines 8-51);

an output selection circuit (fig. 3, ref. 127) coupled to said array of pixels for selecting between the linear output signal and the logarithmic output signal as an output signal (col. 6, lines 8-51).

For **claim 21**, Morris discloses an image sensor (fig. 3, ref. 140) comprising:

an array (119) of pixels (118), each pixel (fig. 4)comprising

a photodiode (152, col. 4, lines 3-29),

a first output circuit (figs. 3, 5, 6,7, 8) connected to said photodiode for generating an output signal to be a linear output signal (col. 4, line 55 – col. 5, line 25; col. 6, lines 32-51), said first output circuit comprising

a reset switch (fig. 3, refs. 124/129) for applying a reset voltage to said photodiode (col. 4, lines 3-29), said reset switch comprising a reset transistor (fig. 4, ref. 150) including a conducting terminal connected to said photodiode (col. 6, lines 32-51), and

a readout switch (fig. 3, refs. 124/129) for turning on the conducting terminal of said reset transistor (col. 4, line 55 – col. 5, line 25; col. 6, lines 8-51). (col. 4, line 55 – col. 5, line 25; col. 6, lines 32-51),

a second output circuit (figs. 3, 9, 10, 11, 12) connected to said photodiode for generating the output signal to be a logarithmic output signal by reading a near instantaneous illumination-dependent voltage on said photodiode that is a logarithmic function of the illumination (col. 5, lines 34-55),), said second output circuit comprises:

an amplifier (fig. 4, ref. 156/160; col. 4, lines 3-54), and

a log select switch (fig. 4, refs. 150/156) for connecting said amplifier to said photodiode (col. 4, lines 30-54; col. 5, line 35 – col. 6, line 51), and

said first and second output circuits sequentially providing the linear and logarithmic output signals (col. 6, lines 8-51); and

an output selection circuit (fig. 3, ref. 127) for selecting between the linear output signal and the logarithmic output signal as an output signal (col. 6, lines 8-51).

For **claim 22**, Morris discloses the image sensor according to claim 21, wherein the linear output signal is selected if the pixel has not saturated during generation of the linear output signal, otherwise, the logarithmic output signal is selected (col. 3, lines 30-46).

For **claim 23**, Morris discloses the image sensor according to claim 21, wherein said first output circuit derives the linear output signal by applying a reset signal to said photodiode and reading a voltage on said photodiode after an integration time (col. 6, lines 32-51).

Claims 25-26 are claims corresponding to the claims 15-16, respectively. Therefore, claims 25-26 are analyzed and rejected as previously discussed with respect to claims 15-16, respectively.

For **claim 31**, Morris teaches a method for operating an image sensor comprising an array of pixels, each pixel comprising a photodiode (col. 4, lines 3-29), the method comprising:

deriving a linear output signal from each pixel (col. 4, line 55 – col. 5, line 25; col. 6, lines 32-51) using a first output circuit comprising a reset switch for applying a reset voltage to said photodiode (col. 4, lines 3-29), said reset switch comprising a reset transistor including a conducting terminal connected to said photodiode (col. 6, lines 32-51), and a readout switch for turning on the conducting terminal of said reset transistor after expiration of the integration time (col. 4, line 55 – col. 5, line 25; col. 6, lines 8-51). (col. 4, line 55 – col. 5, line 25; col. 6, lines 32-51),

deriving a logarithmic output signal from each pixel using a second output circuit by reading a near instantaneous illumination-dependent voltage on the photodiode that is a logarithmic function of the illumination, said second output circuit comprises an amplifier , and a log select switch for connecting said amplifier to said photodiode (col. 4, lines 3-54; col. 5, line 35 – col. 6, line 51), and

sequentially providing the linear and logarithmic output signals (col. 5, lines 34-55); and

selecting between the linear output and the logarithmic output signal as an output signal (col. 6, lines 8-51).

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. **Claims 17 and 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris et al. (U.S. Pat. 6,697,112) in view of in view of Luo et al. (U.S. Pat. 7,071,982).

For **claim 17**, Morris discloses the image sensor according to claim 16, wherein said amplifier is connected to the conducting terminal of said reset transistor. However, Morris does not expressly disclose wherein said amplifier comprises a differential amplifier having an inverting input connected to the conducting terminal of said reset transistor, and a non-inverting input connected to a reference voltage.

In a similar field of endeavor, Luo discloses the image sensor (fig. 2), wherein said amplifier comprises a differential amplifier (36) having an inverting input connected to the conducting terminal of said reset transistor (V_{PH}), and a non-inverting input connected to a reference voltage (V_{REF}). Please read Luo, col. 5, lines 25-46. In light of the teaching of Luo, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the amplifier of Morris with a differential amplifier as claimed in claim 17 in order to improve the image capture efficiency thereby providing an image with increased wide dynamic range as well as improving power consumption (Luo, col. 1, line 63 – col. 2, line 39).

Claim 27 is a claim corresponding to claim 17. Therefore, claim 27 is analyzed and rejected as previously discussed with respect to claim 17.

7. **Claims 18-19, 28-29, and 34-35** are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris et al. (U.S. Pat. 6,697,112) in view of Kusaka et al. (US 2005/0052557).

For **claim 18**, Morris discloses the image sensor according to claim 14. However, Morris does not expressly teach further comprising a calibration circuit for calibrating each pixel before deriving the logarithmic output signal.

In a similar field of endeavor, Kusaka discloses an image sensor (fig. 1, ref. 1) comprising a calibration circuit (fig. 1, refs. 4-6) for calibrating each pixel before deriving the logarithmic output signal (p. 3-4, paragraphs 54-71). Also, please see Kusaka, figs. 2-3. In light of the teaching of Kusaka, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the image sensor of Morris with a calibration circuit as claimed in claim 18 in order to automatically achieve an improved wide brightness range as well as an improved a narrow brightness range (Kusaka, p. 1, paragraphs 7-12).

For **claim 19**, Morris, as modified by Kusaka, discloses the image sensor according to claim 18, wherein said calibrating circuit comprises a constant current source selectively connected to each respective pixel (Kusaka p. 3, paragraph 60; fig. 3).

Claims 28-29 are claims corresponding to the claims 18-19, respectively. Therefore, claims 28-29 are analyzed and rejected as previously discussed with respect to claims 18-19, respectively.

Claims 34-35 are claims corresponding to the claims 18-19, respectively. Therefore, claims 34-35 are analyzed and rejected as previously discussed with respect to claims 18-19, respectively.

8. **Claims 20, 30, and 36** are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris et al. (U.S. Pat. 6,697,112) in view of Kusaka et al. (US 2005/0052557) as applied to claims 19, 29, and 35 above, and further in view of He et al. (US Pat. 6,355,965).

For **claim 20**, Morris, as modified by Kusaka (fig. 3) discloses the image sensor according to claim 19, wherein an output node (Kusaka fig. 3, the node between T1 and T2) is associated with each photodiode, and wherein the linear and logarithmic output signals are derived from the output node (Kusaka, p. 3-4, paragraphs 63-64). However, Morris, as modified by Kusaka, do not expressly disclose said calibration circuit further comprising a switch connected between said photodiode and the output node for isolating said photodiode from the output node while calibration takes place.

In a similar field of endeavor, He discloses a calibration circuit comprising a switch (fig. 4, S2) connected between said photodiode and the output node for isolating said photodiode from the output node while calibration takes place (col. 4, lines4-23). In light of the teaching of He, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the image sensor of Morris, as modified by Kusaka, with a switch as claimed in claim 20 in order to change to calibration mode (He, col. 4, lines4-23).

Both of **claims 30 and 36** are claims corresponding to the claim 20. Therefore, claims 30 and 36 are each analyzed and rejected as previously discussed with respect to claim 20.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carramah J. Quiett whose telephone number is (571)272-7316. The examiner can normally be reached on 8:00-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NgocYen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. J. Q./
Examiner, Art Unit 2622
December 16, 2008

/Ngoc-Yen T. VU/
Supervisory Patent Examiner, Art Unit 2622